

INTEGRATING CIRCUIT SIMULATION WITH EIT FEM MODELS

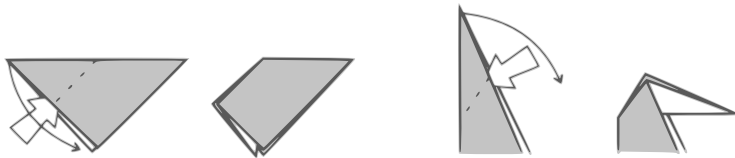
Alistair Boyle and Andy Adler

University of Ottawa
Ottawa, Canada

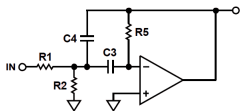
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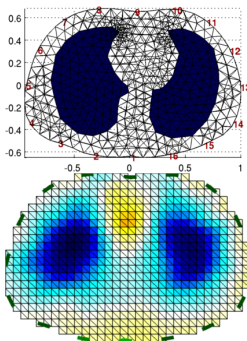
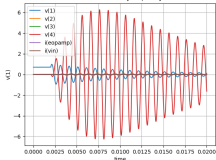
EIT2018, June 11–13, 2018



CIRCUITS AND FEM



1kHz Band-Pass Filter: Transient Analysis (Wed Jun 20 16:02:03 2018)



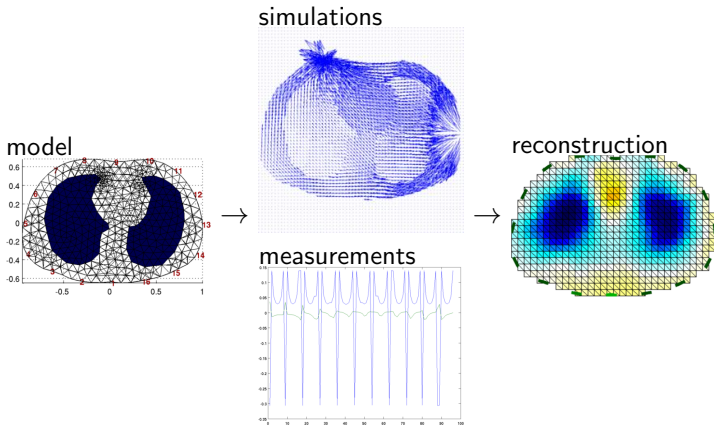
Step 1: forward solution

improve hardware designs with accurate simulations

Step later: inverse solution

handle hardware imperfections and aging

EXAMPLE: EIT

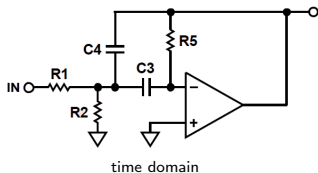
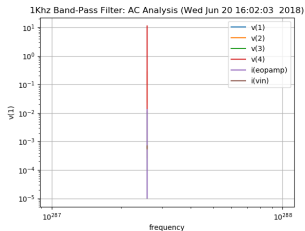


EXAMPLE: CIRCUIT SIMULATION (SPICE)

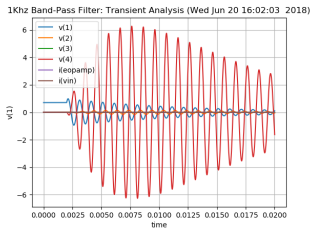
Non-linear circuit analysis (opamps, I/O models) and signal integrity (transmission lines)

```
1kHz Band-Pass Filter
Vin 1 0 DC 0 AC 1
R1 1 2 1.59k
R2 2 0 41
C3 2 3 100nF
C4 2 4 100nF
R5 4 3 1 64k
Eopamp 5 0 0 3 1000
```

frequency domain



time domain



and detailed non-linear semiconductor and IBIS device models

EIT + SPICE

1 EIT → spice

2 EIT ← spice

EIT + SPICE

1 EIT → spice

EIT \rightarrow SPICE

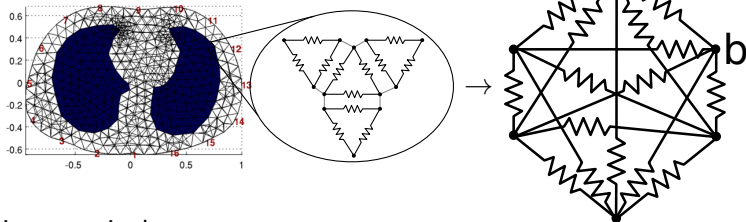
blockwise matrix inverse: a model reduction

$$\begin{bmatrix} \mathbf{V}_A \\ \mathbf{V}_D \end{bmatrix} = \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{B}^\top & \mathbf{D} \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ \mathbf{X}_D \end{bmatrix} \quad (1)$$

$$\mathbf{D}' = \mathbf{D} - \mathbf{B}^\top \mathbf{A}^{-1} \mathbf{B} \quad (2)$$

$$\mathbf{V}_D = \mathbf{D}'^{-1} \mathbf{X}_D \quad (3)$$

EIT \rightarrow SPICE



resistor equivalence:

$$\mathbf{D}' = \mathbf{D} - \mathbf{B}^T \mathbf{A}^{-1} \mathbf{B}$$

- \mathbf{D}' is an N -port full mesh resistor network
- \mathbf{D}' off-diagonal values are $1/R_{ab}$ between electrode a and b
- delta-wye conversion for 2D models, but its not worth the trouble
- complex-valued extension: R to RLC network

General FEM \rightarrow spice methods used in EMI and antenna analysis

EXAMPLE: EIT \rightarrow SPICE (FORWARD SOLUTION)

SPICE input files:

file: stim.s	file: eit.s
Test circuit for EIT	* full-mesh R network of 8-electrode EIT
.inc eit.s	FEM
rgnd e1 0 1e-16	.subckt eit e1 e2 e3 e4 e5 e6 e7 e8
isrc e1 e2 dc 1A	re01 e1 e2 3.9298245614035099
Xeit e1 e2 e3 e4 e5 e6 e7 e8 eit	re02 e1 e3 11.200000000000005
.control	re03 e1 e4 21.000000000000018
print V(e1,e2) V(e2,e3) V(e3,e4)	[...]
+ V(e4,e5) V(e5,e6) V(e6,e7)	re25 e5 e8 21.000000000000018
+ V(e7,e8) v(e8,e1)	re26 e6 e7 1.58490566603773584
.endc	re27 e6 e8 11.200000000000008
.end	re28 e7 e8 3.9298245614035099
	.ends

EIDORS output:

-1.6239
0.4517
0.2500
0.0483
0.1239
0.0483
0.2500
0.4517

==

SPICE output:

Circuit: test circuit for eit
[...]
v(e1,e2) = -1.62395e+00
v(e2,e3) = 4.516807e-01
v(e3,e4) = 2.500000e-01
v(e4,e5) = 4.831933e-02
v(e5,e6) = 1.239496e-01
v(e6,e7) = 4.831933e-02
v(e7,e8) = 2.500000e-01
v(e8,e1) = 4.516807e-01

EIT + SPICE

2 EIT ← spice

SPICE \rightarrow EIT

Input: SPICE netlist

Modified Nodal Analysis (MNA) circuit analysis ideal elements:

2 node elements

- “Rn” resistor
- “Cn” capacitor
- “Ln” inductor
- “Vn” voltage source
- “In” current source

4 node elements

- “En” voltage controlled voltage source (VCVS)
- “Fn” current controlled current source (CCCS)
- “Gn” voltage controlled current source (VCCS)
- “Hn” current controlled voltage source (CCVS)

$$\text{ind: } \begin{bmatrix} -1/sL & 1/sL \\ 1/sL & -1/sL \end{bmatrix} \begin{bmatrix} V_+ \\ V_- \end{bmatrix} \quad \text{VCVS: } \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & +1 \\ 0 & 0 & 0 & 0 & 0 \\ G & -1 & 1 & -G & 0 \end{bmatrix} \begin{bmatrix} V_{i+} \\ V_{o+} \\ V_{o-} \\ V_{i-} \\ I_o \end{bmatrix}$$

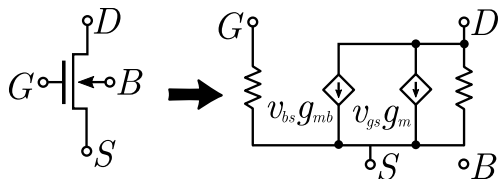
$$s = j\omega$$

Grounded nodes are a special case

We use the FEM connectivity matrix to “stitch” nodes in FEM (electrodes) to circuit nodes

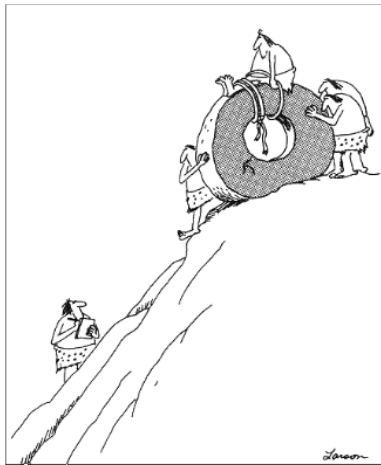
STEP LATER: INVERSE PROBLEM

Nonlinear components (opamp, diode, transmission line, transistor) modelled by linearizing to ideal components



SPICE implementations provide algorithms to find operating points for small signal nonlinear models, including those that exhibit hysteresis (ex. Schmitt triggers)

CHALLENGES



Early experiments in transportation

¹ ©Gary Larson, The Farside

CHALLENGES

On the failure of the Cadence Spectre SPICE simulator to penetrate the market, despite being faster, more accurate, more robust:

*[... we] completed the first version in two weeks [...] One can find serious faults in any SPICE simulator you try. Ironically, the faults are one of the things that make it hard to replace.*²

- HSpice *Synopsys*
- PSpice *Cadence*
- Spectre *Cadence*
- LTspice IV *Linear Technologies*
- TINA *Texas Instruments*
- 5Spice *Cadence*
- SuperSpice *AnaSoft*
- NI Multisim *National Instruments*
- TopSpice *Penzar*
- ngSpice *GPL*
- EveryCircuit *MuseMaze*
- Qucs *GPL*

²K. Kundert (2011) *The Life After Spice*, IEEE Solid-State Circuits Magazine

POSSIBLE DIRECTIONS

1 EIT → spice

- support grounding current
- complex-valued conductivities (RLC networks)
- time/frequency-dependent models

2 EIT ← spice

- SPICE library integration^a (ngspice)
- solve inverse problem for circuit parameters

^anot with matlab

AVAILABLE NOW AT A CODE REPOSITORY NEAR YOU

1 EIT → spice

- for real-valued conductivities
- at a single-frequency
- generates “standard” spice netlist (sub-circuit)
- `eidors/solvers/forward/eit_spice.m`

2 EIT ← spice

- parses “standard” spice netlist
- for linear circuits
- forward model^a
- `eidors/solvers/forward/spice_eit.m`

^aMNA “stitching” not yet implemented